L Number	Hits	Search Text	DB	Time stamp
1	4	(("6075932") or ("6151568") or ("6321185") or ("6363515")).PN.	USPAT	2004/10/13 18:43

L Number	Hits	Search Text	DB	Time stamp
11	1742	((716/4) or (716/18) or (716/14)).CCLS.	USPAT	2004/10/13 18:05
13	1	((((716/4) or (716/18) or (716/14)).CCLS.) and (power same model) and rtl) and (high adj level adj language) same instruction	USPAT	2004/10/13 18:06
14	1	((((716/4) or (716/18) or (716/14)).CCLS.) and (power same model) and rtl) and ((high adj level adj language) same instruction)	USPAT	2004/10/13 18:06
12	66	(((716/4) or (716/18) or (716/14)).CCLS.) and (power same model) and rtl	USPAT	2004/10/13 18:10
15	106	(703/18).CCLS.	USPAT	2004/10/13 18:10
16	5	((703/18).CCLS.) and (power same model) and rtl	USPAT	2004/10/13 18:11

L Number	Hits	Search Text	DB	Time stamp
1	8881	(hardware same software) and instruction$2 and (simulator or simulation)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/13 13:29
2	1220	((hardware same software) and instruction$2 and (simulator or simulation)) and dependency	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/13 13:29
3	519	(((hardware same software) and instruction$2 and (simulator or simulation)) and dependency) and power and (usage or consumption)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/13 13:30
4	2	((((hardware same software) and instruction$2 and (simulator or simulation)) and dependency) and power and (usage or consumption)) and (capture$2 same (gate-level or gate adj level))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/13 13:36
5	31	refine same (data adj model)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/13 13:47
6	0	refine same ((power or energy) near model)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/13 13:47
7	113	refine same ((power or energy) and model)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/13 13:48
8	28	(refine same ((power or energy) and model)) and SOC	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/13 13:50
9	40330	model same (change or modification or refinement)	USPAT	2004/10/13 13:50
10	1281	model adj (change or modification or refinement)	USPAT	2004/10/13 13:51
11	66	(model adj (change or modification or refinement)) and (power adj consumption)	USPAT	2004/10/13 14:30
12	9	US-5481469-$.DID. OR US-5870308-$.DID. OR US-5572436-$.DID. OR US-5801958-$.DID. OR US-5696694-$.DID. OR US-5682320-$.DID. OR US-5838579-$.DID. OR US-5838947-$.DID. OR US-5903476-$.DID.	USPAT	2004/10/13 14:31
13	23	manually adj optimize	USPAT	2004/10/13 15:18

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1 **Instruction-based system-level power evaluation of system-on-a-chip peripheral cores**
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Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 6 , Dec. 2002
Pages:856 - 863

[Abstract] [PDF Full-Text (455 KB)] **IEEE JNL**

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[Abstract] [PDF Full-Text (644 KB)] **IEEE CNF**

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Pages:306 - 311

[Abstract] [PDF Full-Text (504 KB)] **IEEE CNF**

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4 **Evaluation of architecture-level power estimation for CMOS RISC processors**
Sato, T.; Ootaguro, Y.; Nagamatsu, M.; Tago, H.;
Low Power Electronics, 1995., IEEE Symposium on , 9-11 Oct. 1995
Pages:44 - 45

[Abstract] [PDF Full-Text (172 KB)] **IEEE CNF**

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5 **A retargetable VLIW compiler framework for DSPs with instruction-level**

parallelism
Rajagopalan, S.; Rajan, S.P.; Malik, S.; Rigo, S.; Araujo, G.; Takayama, K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 20 , Issue: 11 , Nov. 2001
Pages:1319 - 1328

[Abstract] [PDF Full-Text (200 KB)] **IEEE JNL**

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6 **Power analysis of embedded software: a first step towards software power minimization**
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Pages:437 - 445

[Abstract] [PDF Full-Text (912 KB)] **IEEE JNL**

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7 **SEA: fast power estimation for micro-architectures**
Kalla, P.; Henkel, J.; Xiaobo Sharon Hu;
ASIC, 2003. Proceedings. 5th International Conference on , Volume: 2 , 21-24 Oct. 2003
Pages:1200 Vol.2

[Abstract] [PDF Full-Text (316 KB)] **IEEE CNF**

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8 **Instruction level power analysis and optimization of software**
Tiwari, V.; Malik, S.; Wolfe, A.; Lee, M.T.-C.;
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Pages:326 - 328

[Abstract] [PDF Full-Text (368 KB)] **IEEE CNF**

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9 **Deterministic clock gating for microprocessor power reduction**
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The Ninth International Symposium on High-Performance Computer Architecture, 2003. HPCA-9 2003. Proceedings. , 8-12 Feb. 2003
Pages:113 - 122

[Abstract] [PDF Full-Text (350 KB)] **IEEE CNF**

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10 **Exploiting reconfigurability for low-power control of embedded processors**
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Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on , Volume: 5 , 25-28 May 2003
Pages:V-421 - V-424 vol.5

[Abstract] [PDF Full-Text (356 KB)] **IEEE CNF**

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Pages:301 - 305 vol.1

[Abstract] [PDF Full-Text (556 KB)] **IEEE CNF**

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12 **Microprocessor power analysis by labeled simulation**

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Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001. Proceedings , 13-16 March 2001
Pages:182 - 189

[Abstract] [PDF Full-Text (604 KB)] **IEEE CNF**

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13 **Instruction level power model of microcontrollers**
Chakrabarti, C.; Gaitonde, D.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on , Volume: 1 , 30 May-2 June 1999
Pages:76 - 79 vol.1

[Abstract] [PDF Full-Text (348 KB)] **IEEE CNF**

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14 **Exploring optimal cost-performance designs for Raw microprocessors**
Moritz, C.A.; Yeung, D.; Agarwal, A.;
FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium on , 15-17 April 1998
Pages:12 - 27

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

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1 **Implementation of complete AC servo control in a low cost FPGA and subsequent ASSP conversion**
Takahashi, T.; Goetz, J.;
Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE , Volume: 1 , 2004
Pages:565 - 570 Vol.1

[Abstract] [PDF Full-Text (1623 KB)] **IEEE CNF**

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2 **A VHDL-based methodology to develop high performance servo drivers**
Pimentel, J.C.G.; Le-Huy, H.;
Industry Applications Conference, 2000. Conference Record of the 2000 IEEE , Volume: 3 , 8-12 Oct. 2000
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[Abstract] [PDF Full-Text (676 KB)] **IEEE CNF**

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3 **A 3.3-V power adaptive 1244/622/155 Mbit/s transceiver for ATM, SONET/SDH**
Belot, D.; Dugoujon, L.; Dedieu, S.;
Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 7 , July 1998
Pages:1047 - 1058

[Abstract] [PDF Full-Text (368 KB)] **IEEE JNL**

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4 **MPEG-4 video codec on an ARM core and AMBA**
Park, J.H.; Kim, I.K.; Kim, S.M.; Park, S.M.; Koo, B.T.; Shin, K.S.; Seo, K.B.; Cha, J.J.;
MPEG-4. 2001 Proceedings of Workshop and Exhibition on , 18-20 June 2001
Pages:95 - 98

[Abstract] [PDF Full-Text (433 KB)] **IEEE CNF**

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5 **A methodology for the design of application specific instruction set processors (ASIP) using the machine description language LISA**
Hoffmann, A.; Schliebusch, O.; Nohl, A.; Braun, G.; Wahlen, O.; Meyr, H.;

Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM International Conference on , 4-8 Nov. 2001
Pages:625 - 630

[Abstract] [PDF Full-Text (695 KB)] **IEEE CNF**

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2 **An FPGA based digital radar receiver for soft radar**
Walke, R.L.; Dudley, J.; Sadler, D.;
Signals, Systems and Computers, 2000. Conference Record of the Thirty-Fourth Asilomar Conference on , Volume: 1 , 29 Oct.-1 Nov. 2000
Pages:73 - 77 vol.1

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